$$t21 = So$$

$$t22 = So \times 1/4$$

$$t23 = So \times 1/8$$

$$t24 = So \times 1/32 \quad (6)$$

The adder unit 59 adds the data **t1, t2** from the bit compensation unit 58 and outputs the cumulative results **t10, t20** within the predetermined limit of the bit value input to the input buffer unit 33, which can be expressed by the following arithmetic expressions:

$$t10 = t11 + t12 + t13 + t14$$

$$t20 = t21 + t22 + t23 + t24 \quad (7)$$

FIG. 5 is a flowchart for showing the steps of the division and multiplication selection of the division and multiplication selection unit 51. First, the division and multiplication selection unit 51 receives the predetermined number of stages **n** and the scale count **Sc** (step S61). Next, the division and multiplication selection unit 51 compares the bit value of the predetermined number of stages **n** with the bit value of the scale count **Sc** (step S63). If the predetermined number of stages **n** is greater than the scale count **Sc**, then the bit value of the scale count **Sc** is subtracted from the bit value of the predetermined number of stages **n,** yielding a difference value **L** and setting the selection signal to the division operation (step S65).However, if the predetermined number of stages **n** is less than the scale count **Sc**, then the bit value of the predetermined number of stages **n** is subtracted from the bit value

of the scale count **Sc**, yielding the difference value **L** and setting the selection signal to the multiplication operation (step S67).

FIG. 6 is a flowchart for showing the steps of the coefficient calculation performed by the coefficient calculation unit 53 of FIG. 4. First, the coefficient calculation unit 53 receives both the difference value **L**, i.e., the difference between the bit value of the predetermined number of stages **n** and the bit value of the scale count **Sc** (step S71). Next, the coefficient calculation unit 53 calculates the quotient **Q** and the remainder ***R*** by dividing the difference value **L** by ***2*** (step S73). Then the quotient **Q** is outputted to the division and multiplication calculation unit 57, while the remainder ***R*** is outputted to the bit compensation unit 58 (step S75).

FIG. 7 is a flowchart for showing the steps of the division and multiplication performed by the division and multiplication calculation unit 57 of FIG. 4. First, the division and multiplication calculation unit 57 receives data **Si** (output from the second operation unit 55), the quotient **Q** (output from the coefficient calculation unit 53) and the selection signal **D** (output from the division and multiplication selection unit 51) (step S81). Next, the division and multiplication calculation unit 57 determines whether the selection signal **D** is for the division operation or for the multiplication operation based on the received data (step S83). If the selection signal **D** is for the division operation **D1**, the division and multiplication calculation unit 57 divides the data **Si** (output from the second operation unit 55) by 2^{Q}, yielding a result value **So** (step S85). On the other hand, if the selection signal **D** is not for the division

operation, the division and multiplication calculation unit 57 multiplies the data **Si** (output from the second operation unit 55) by 2^{Q}, yielding a result value **So** (step S87).

FIG. 8 is a flowchart for showing the steps of the compensation of bit signal performed by the bit compensation unit 58. First, the bit compensation unit 58 receives the selection signal **D** (output from the division and multiplication selection unit 51), the remainder **R** (output from the coefficient calculation unit 53) and the bit signal **So** (output from the division and multiplication calculation unit 57) (step S81). Next, the bit compensation unit 58 determines whether the remainder **R** is "**1**" (step S83). If the remainder **R** is not "**1**", then the bit compensation unit 58 outputs the bit signal **So** output from the division and multiplication unit 57 intact (step S95).

When the remainder **R** is "**1**", then it is determined whether the selection signal **D** is for the division operation, **D1**, or the multiplication operation, **D2** (step S97). If the selection signal **D** is set for the division operation **D1**, then the bit compensation unit 58 performs the multiplication operation on the bit signal **So** output from the division and multiplication calculation unit 57, outputting result values **t11 = So x 1/2, t12 = So x 1/8, t13 = So x 1/16, t14 = So x 1/64**, respectively (step S98).

On the other hand, if the selection data **D** is for the multiplication operation **D2**, then the bit compensation unit 58 performs the multiplication operations on the bit signal **So** output from the division and multiplication